.....

Fig.1 (Prior Art)

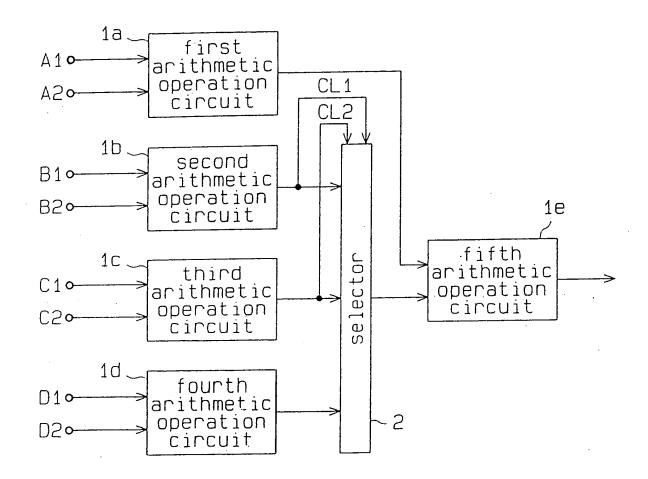


Fig.2

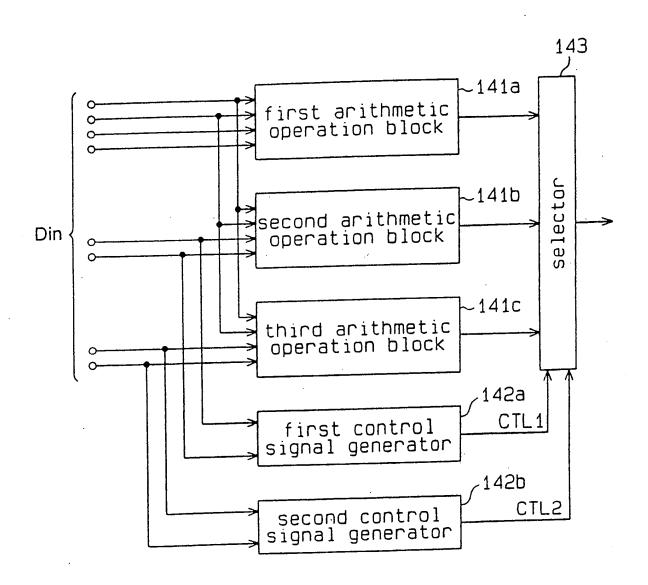


Fig.3

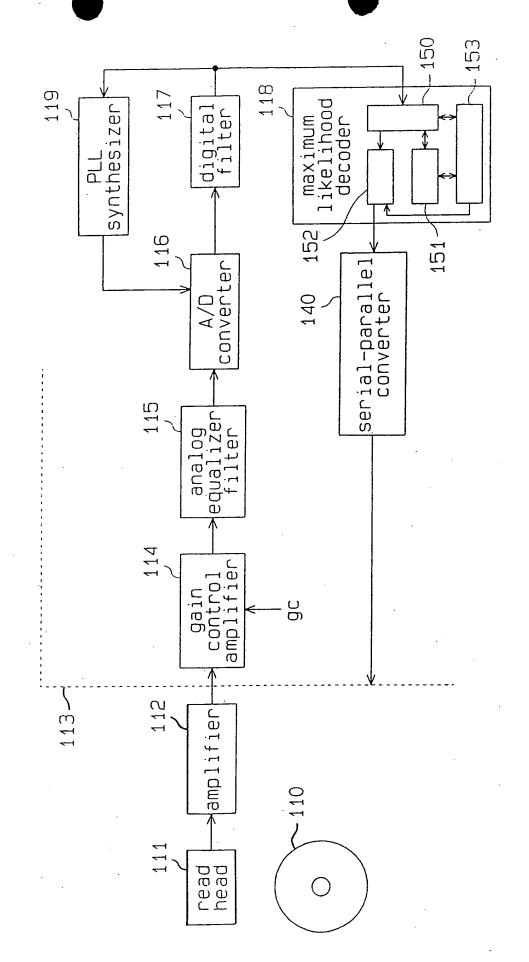


Fig.4

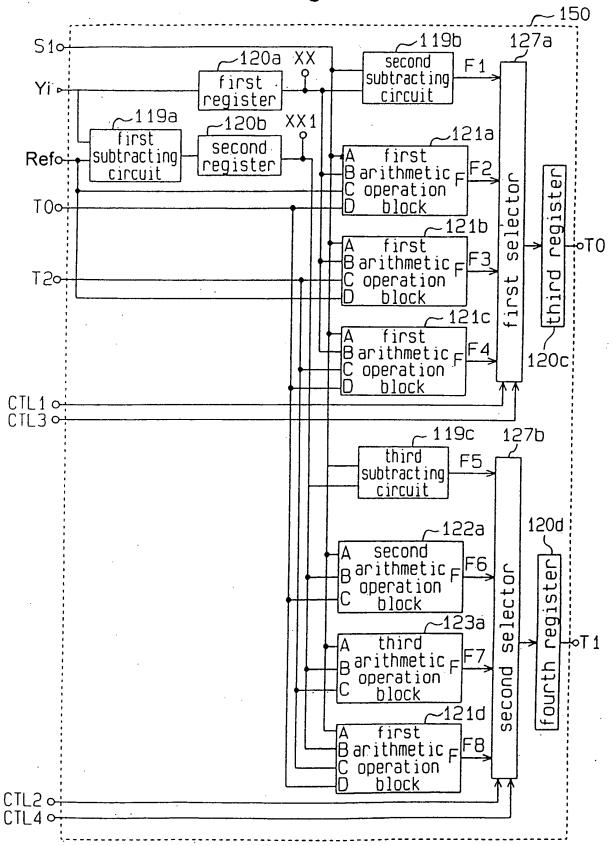
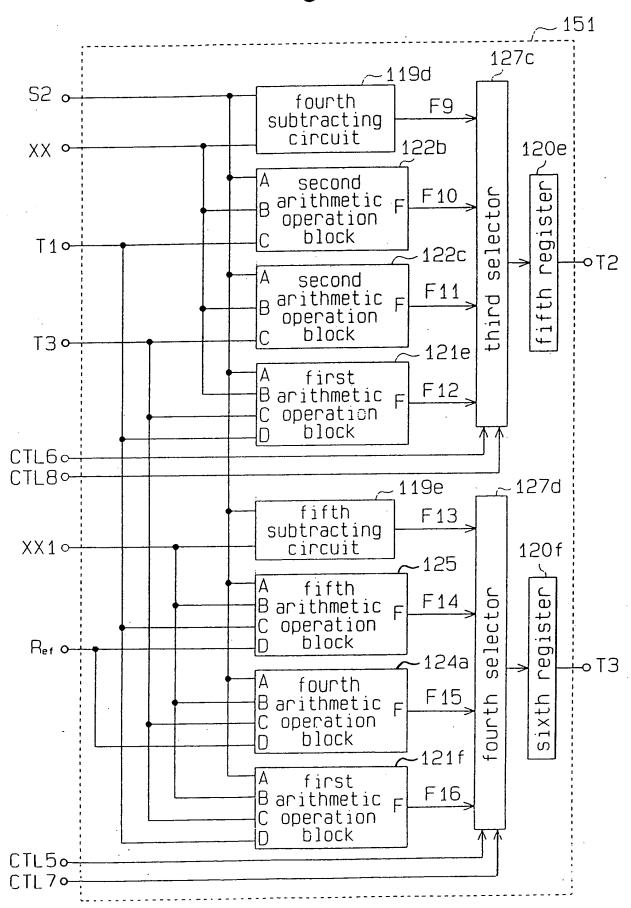


Fig.5



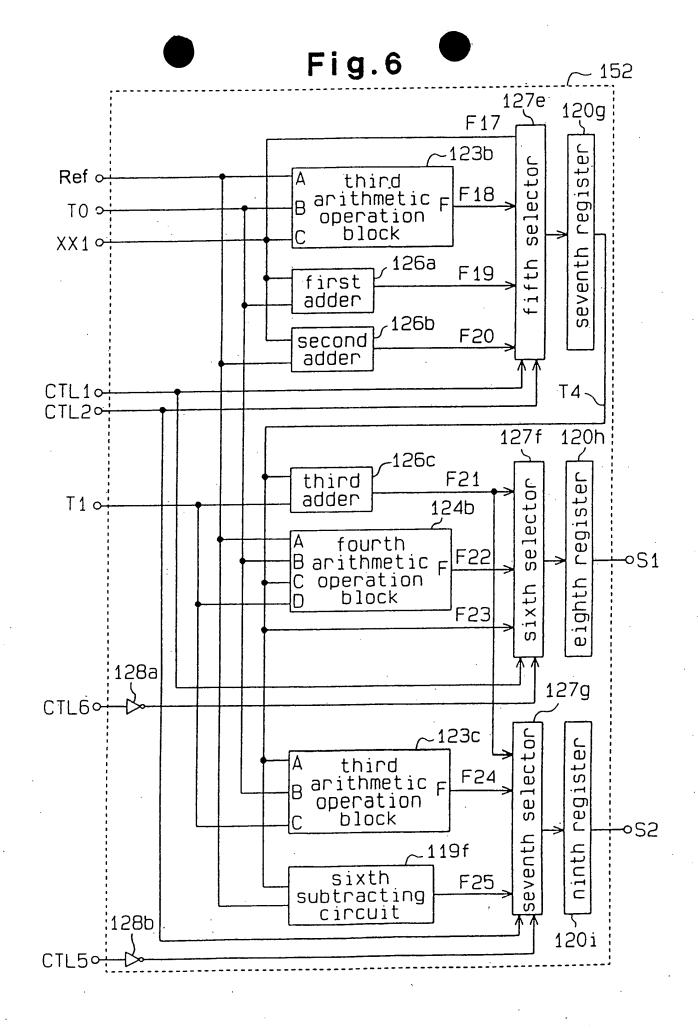


Fig.7

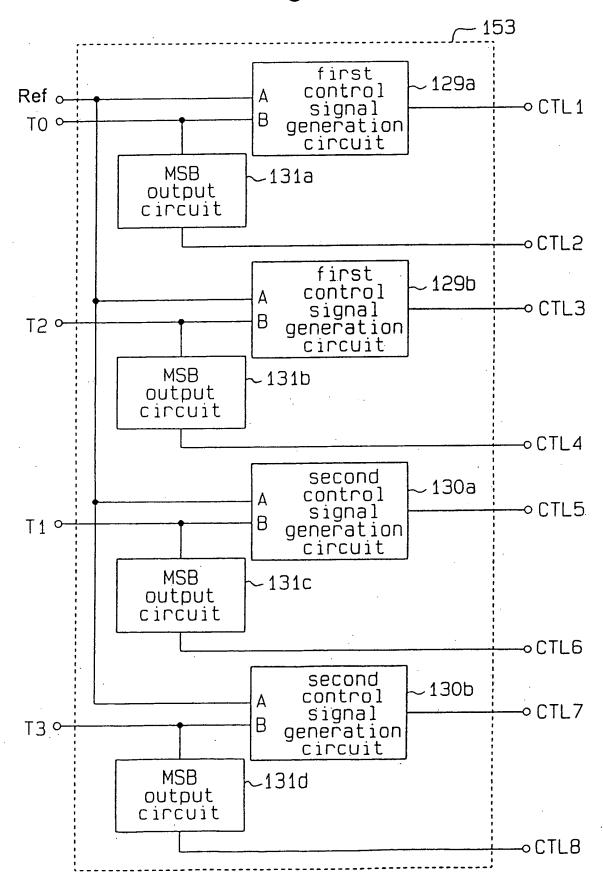
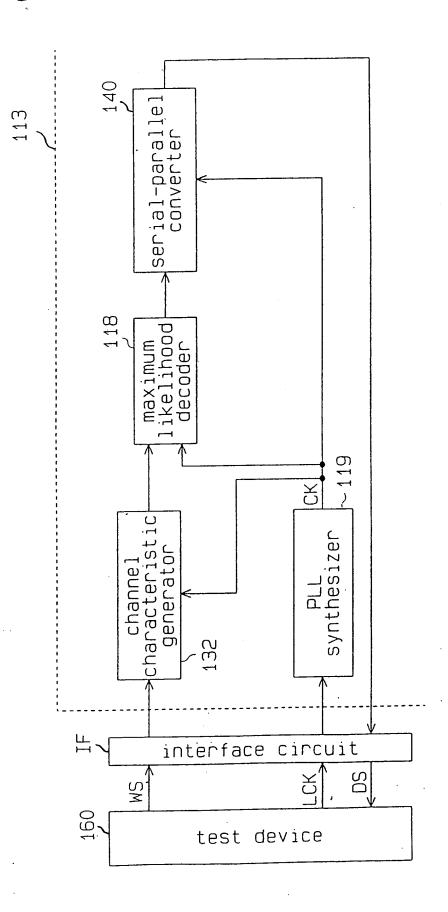
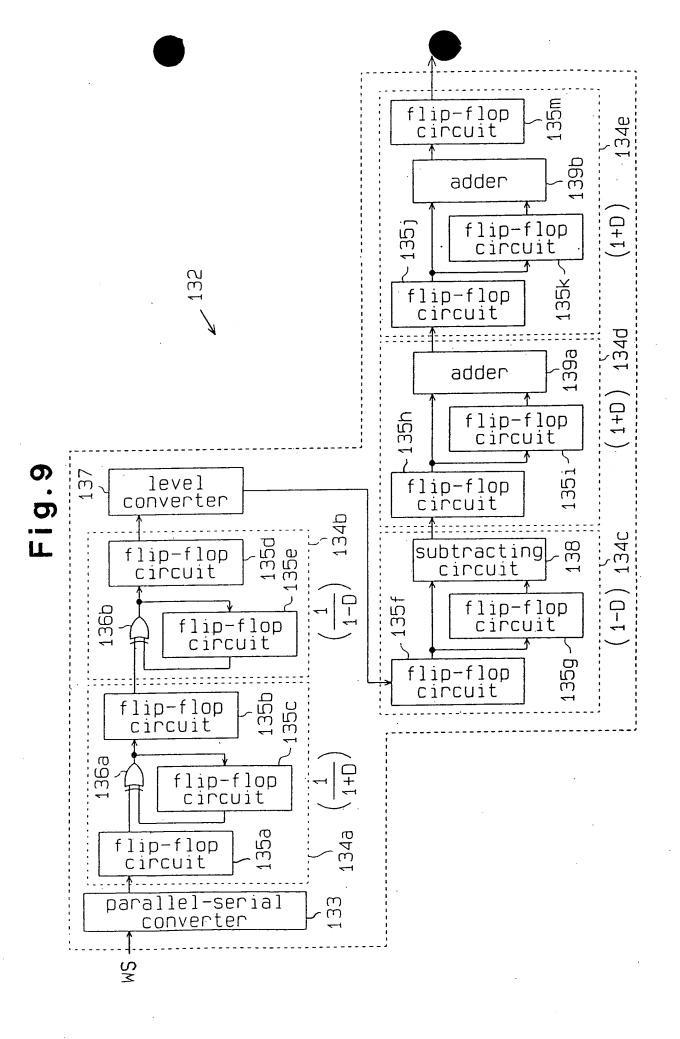
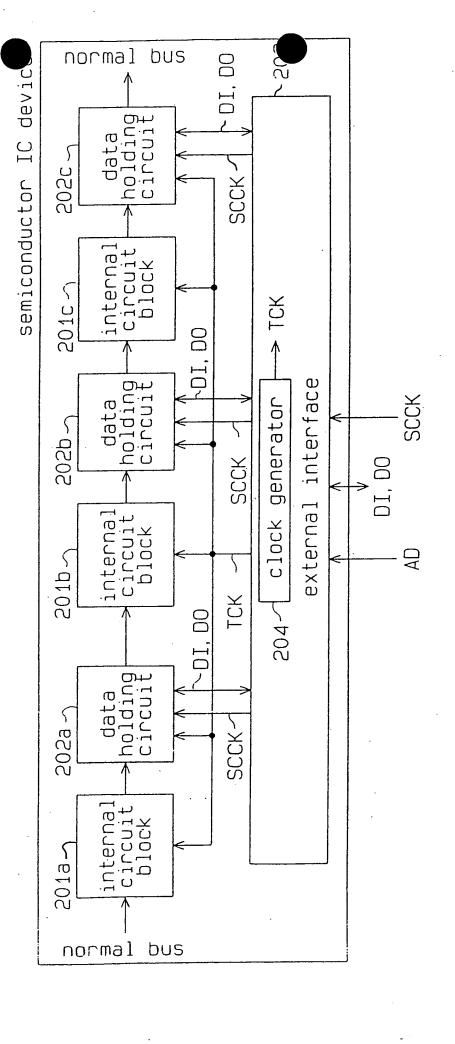
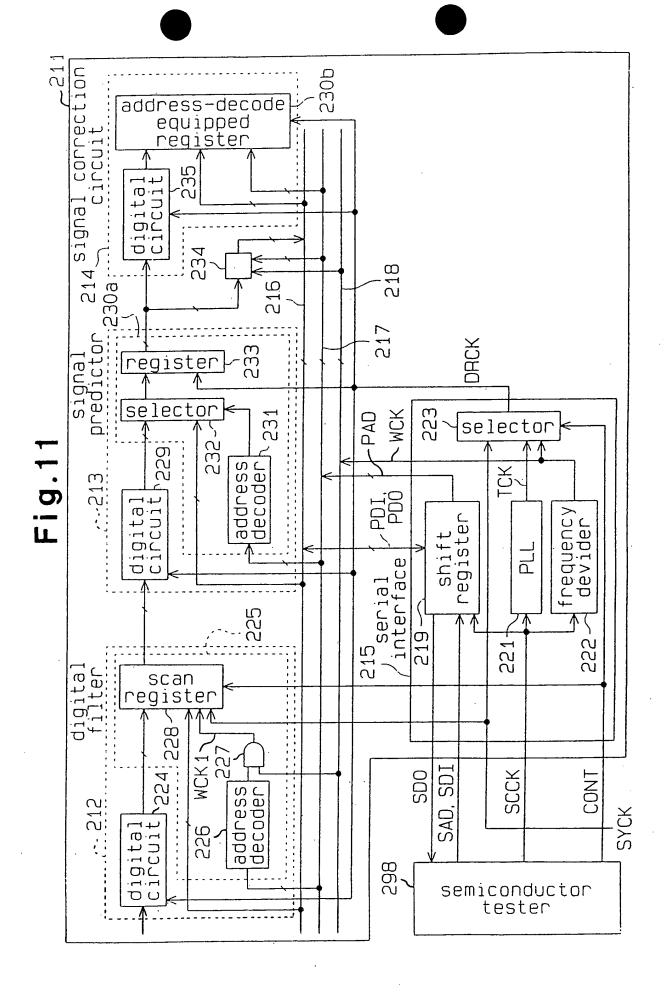


Fig.8





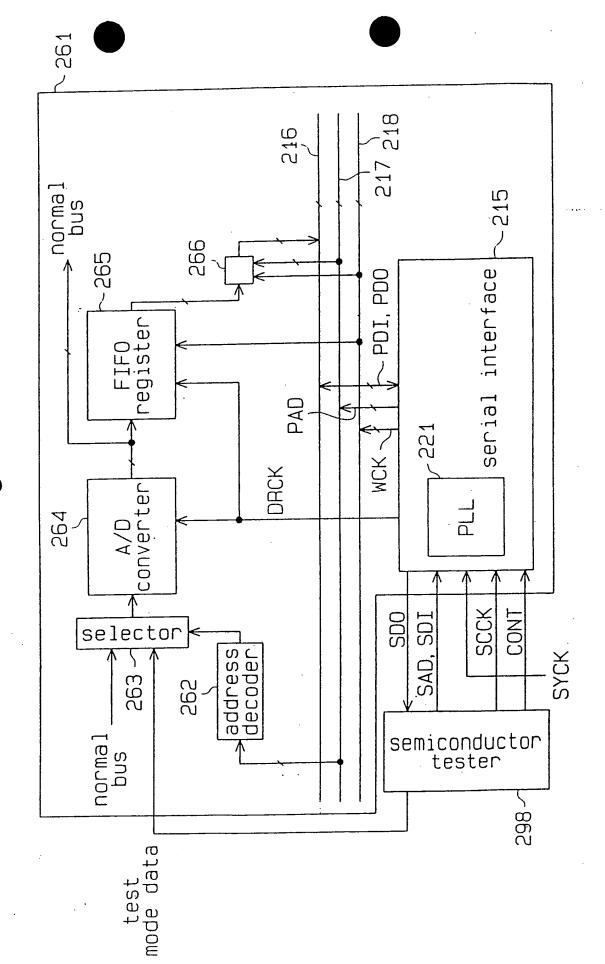




-236 240 normal bus 217218 -296 216 239 215 predictor 244 bus memory 298 / 297 serial interface PD0 signal \ DRCK metric arithmetic operation circuit PDI, Fig.12 237 -221 243 PLL PAD MCK selector address 242/ SCCK SDO CONT SDI 241 SYCK SAD, semiconductor tester 298 normal bus 238 298~ 296. 297

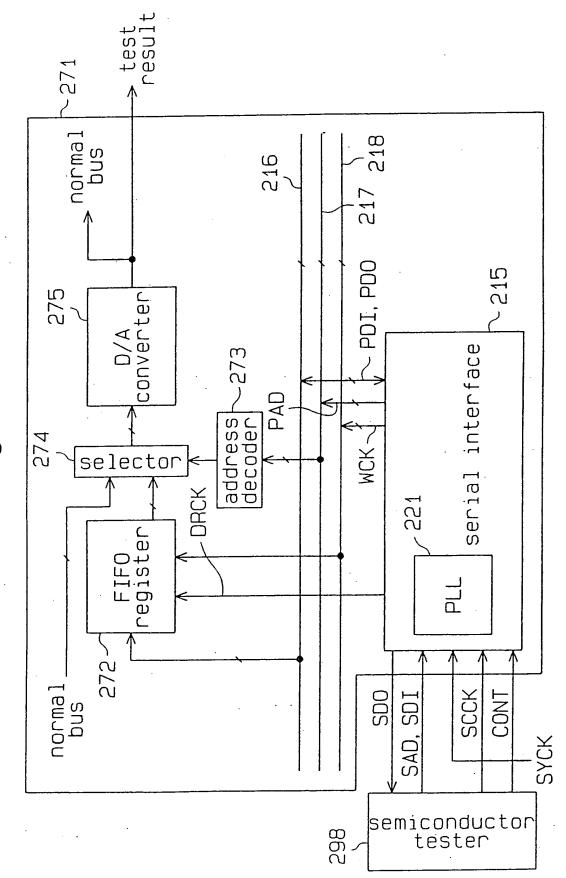
AN

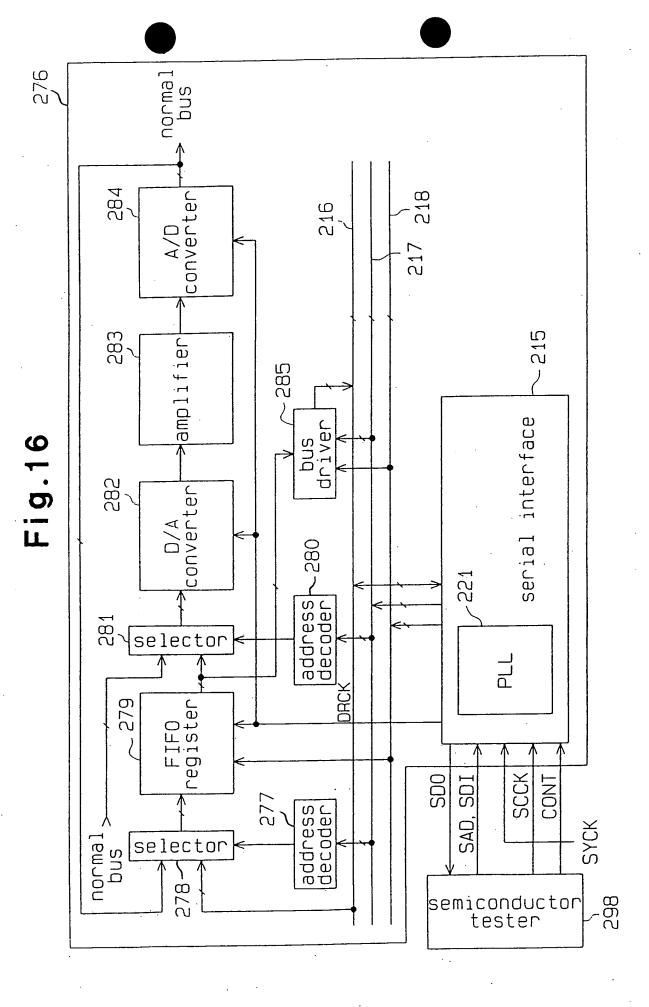
Fig.14



M.

Fig.15





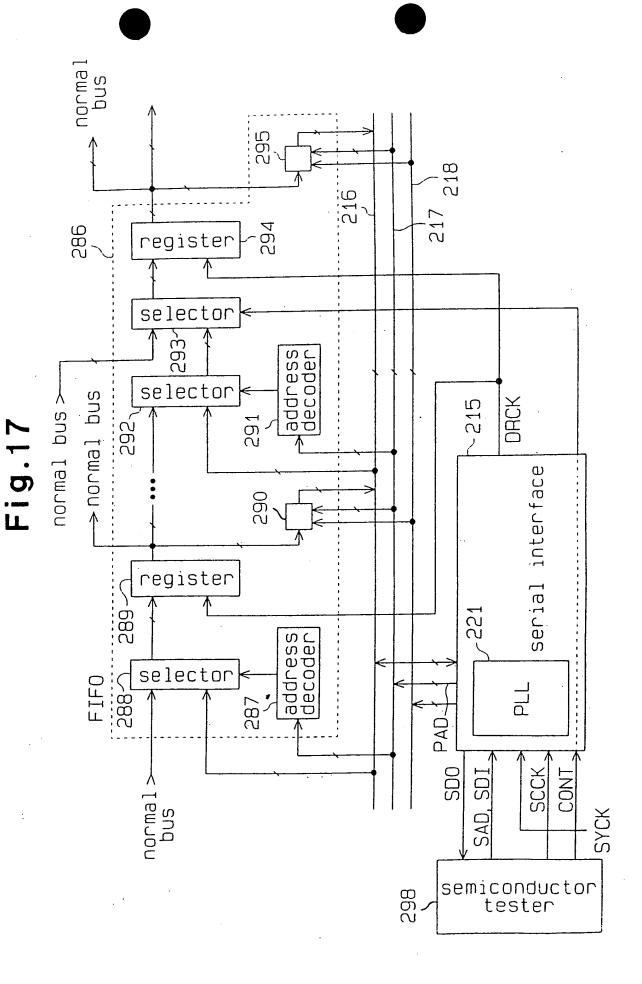


Fig.18

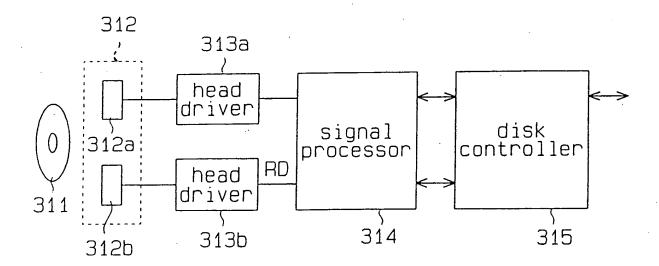
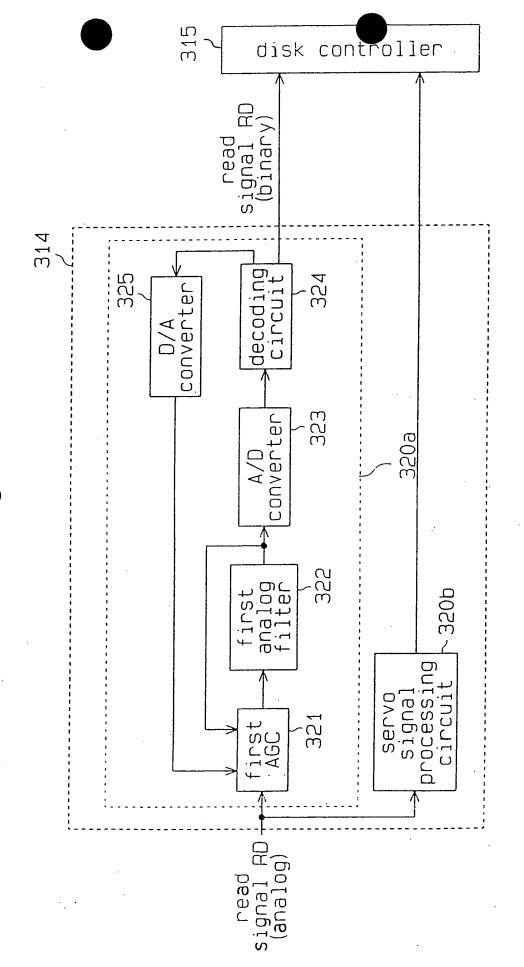
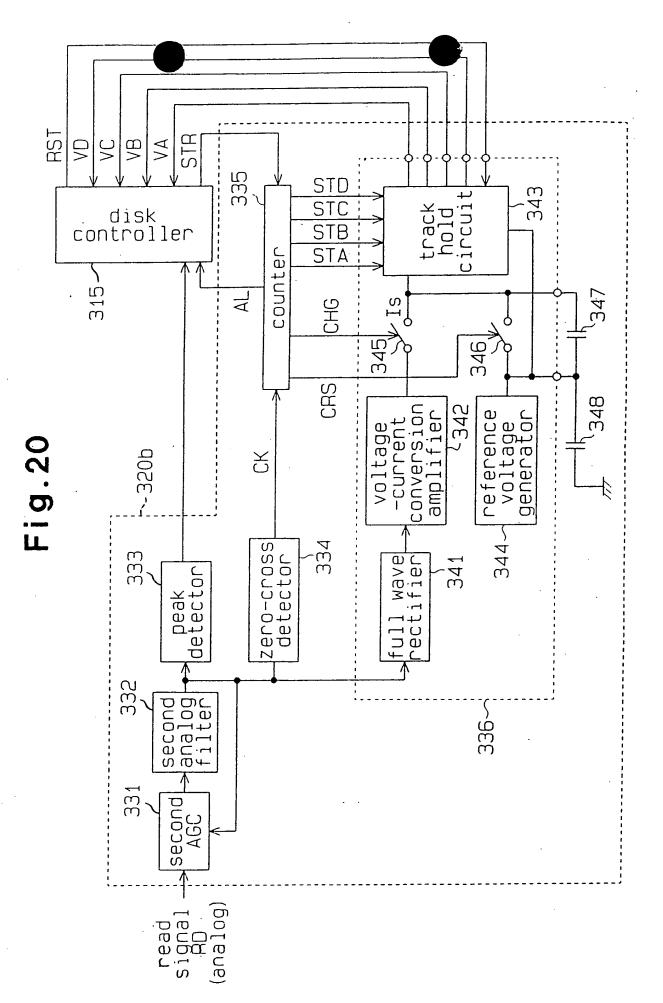


Fig.19





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Fig. 21

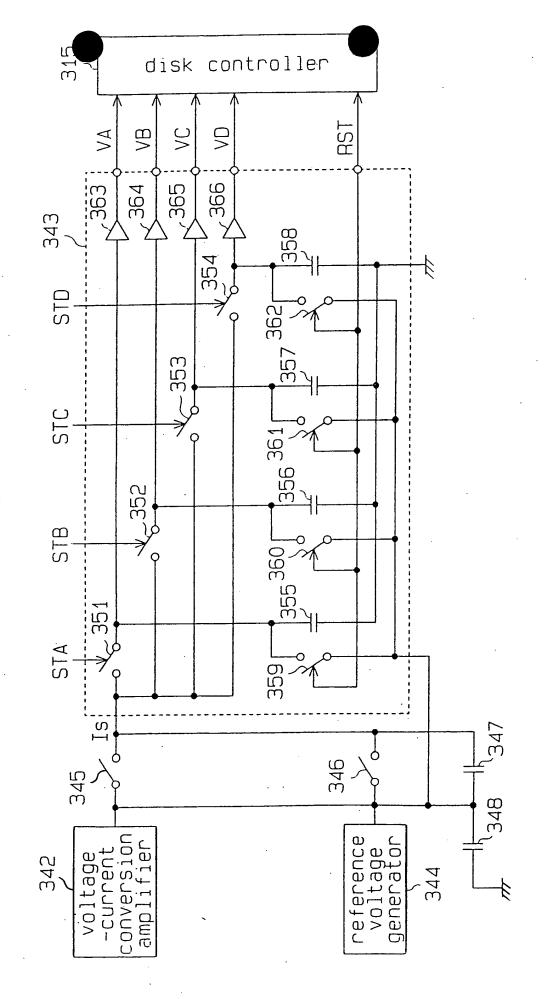


Fig. 22

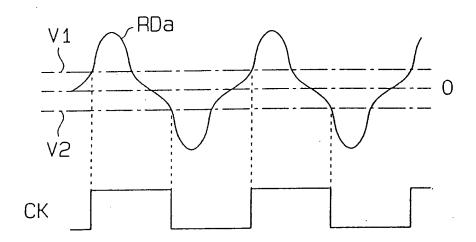


Fig.23

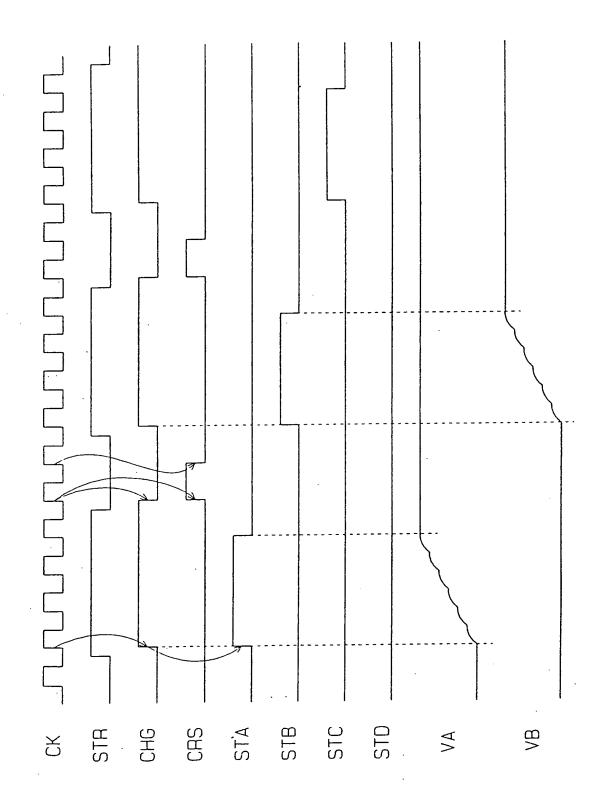
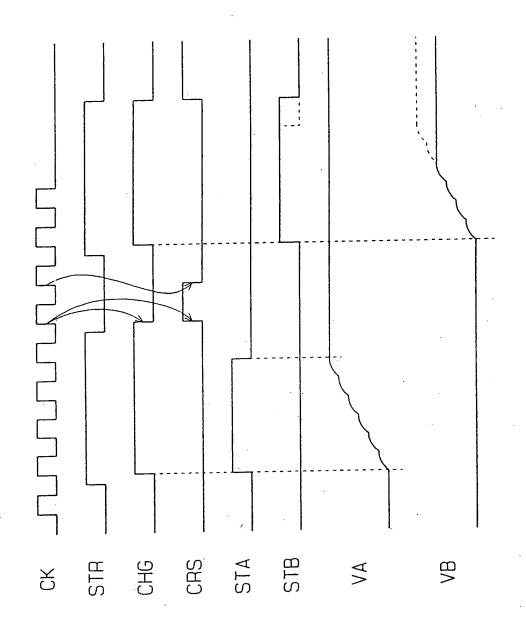


Fig. 24



1 14 14 . . .

Fig. 25

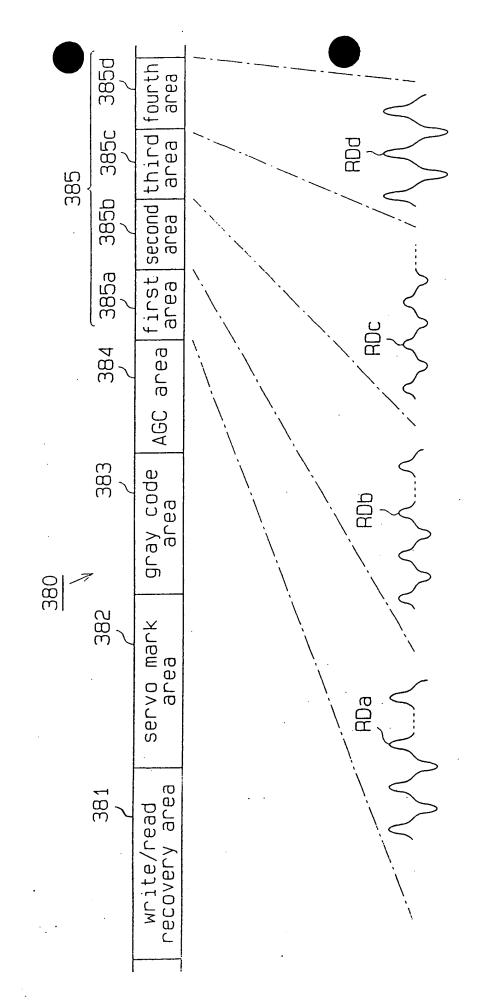


Fig. 26

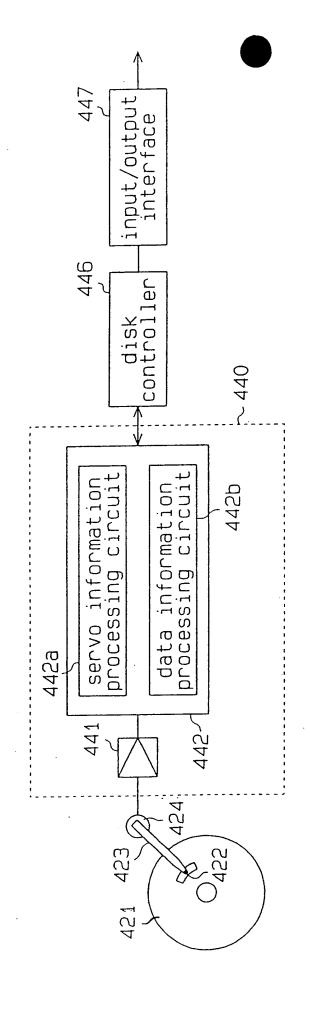
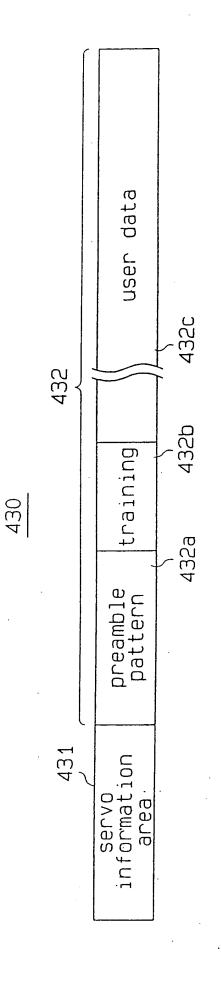


Fig. 27



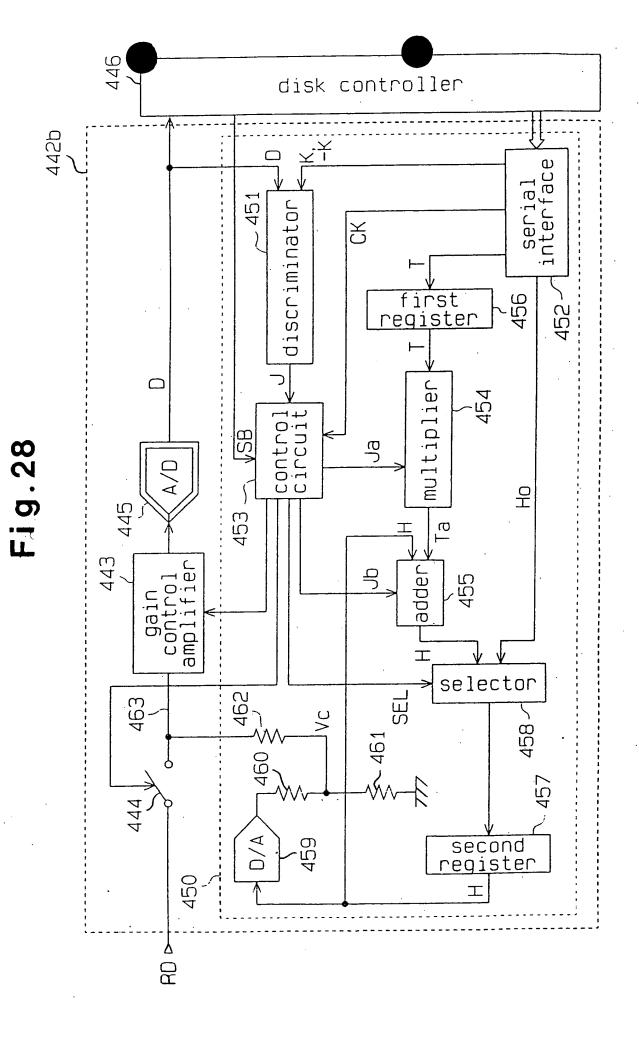
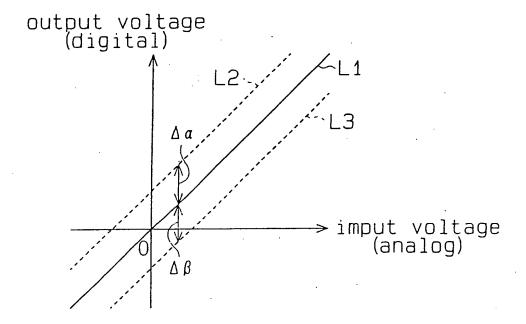


Fig.29



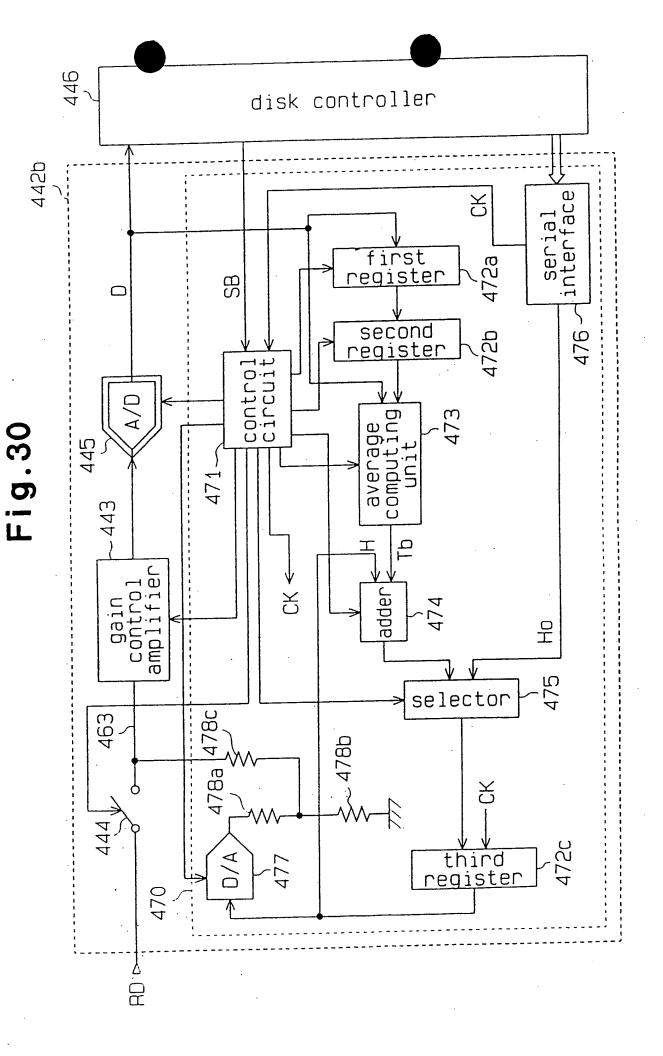


Fig. 31

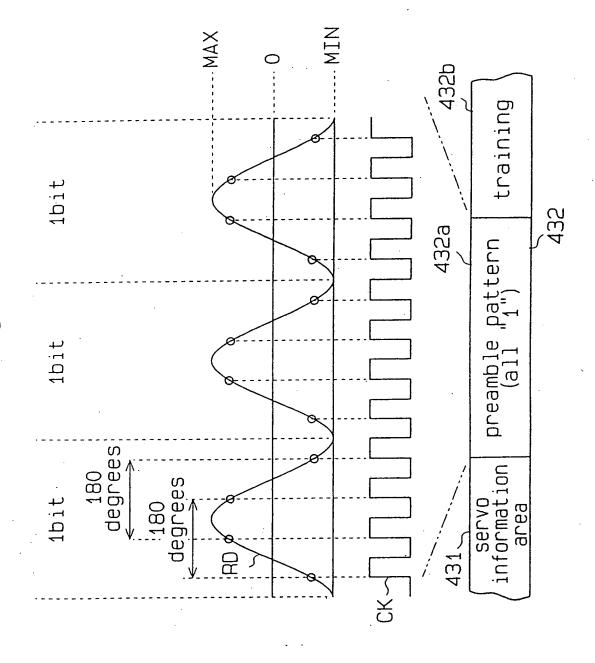


Fig.32

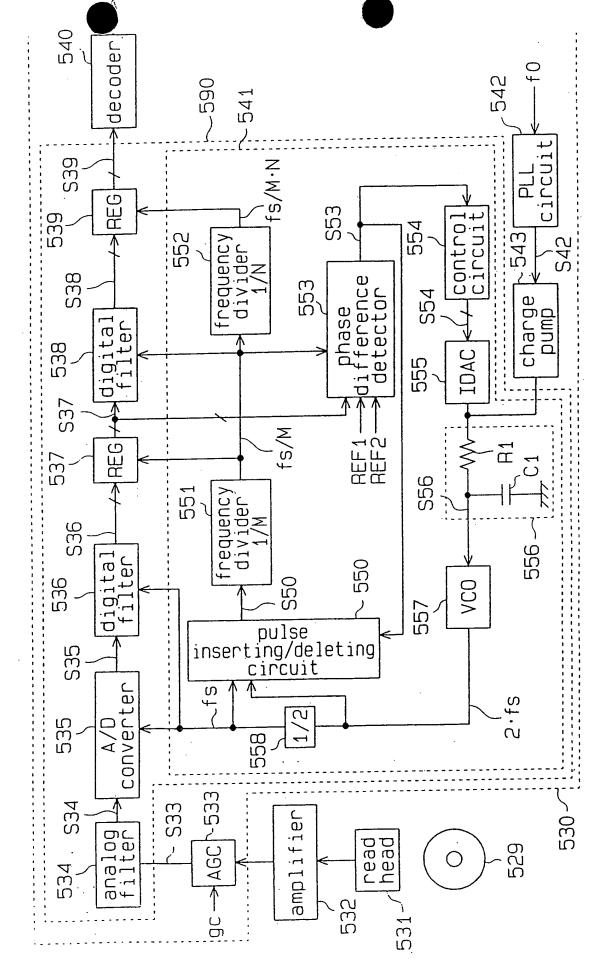
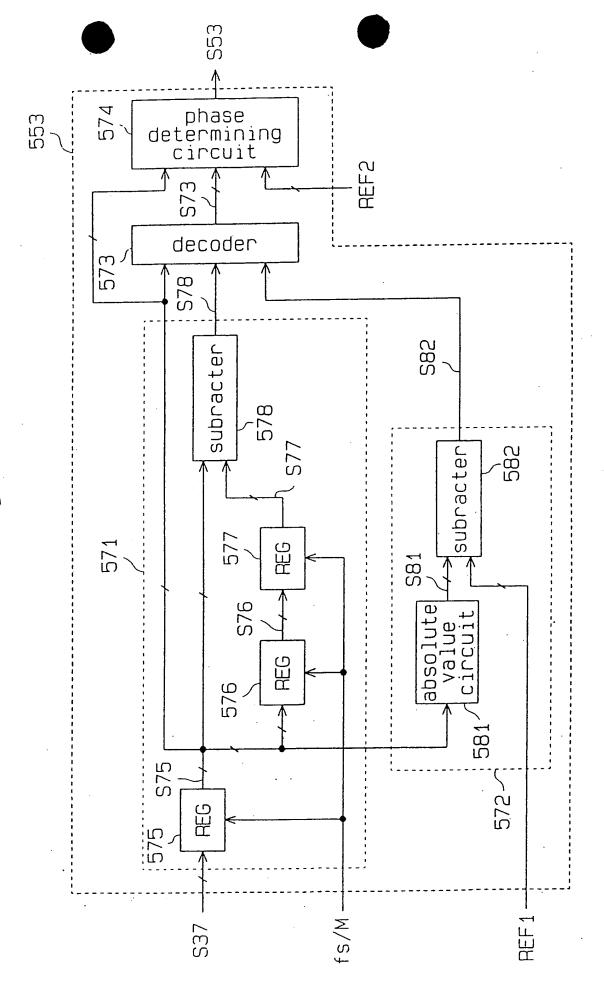
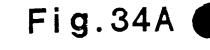


Fig. 33





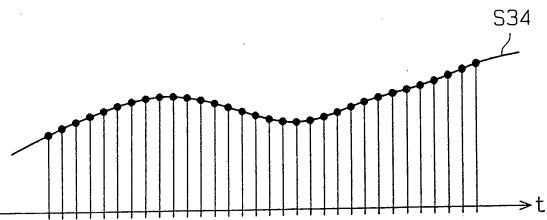


Fig.34B

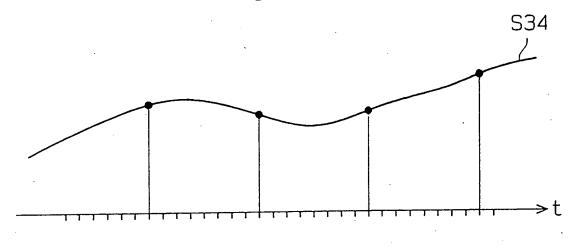
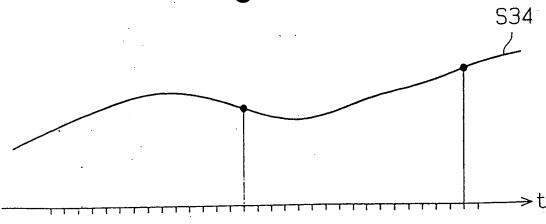


Fig.34C



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Fig.35

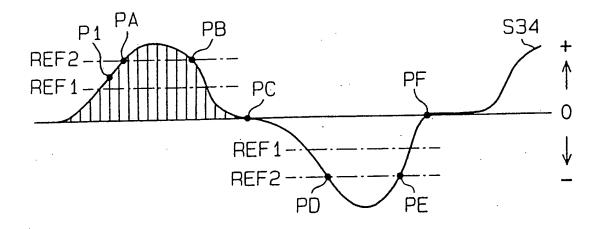


Fig.36

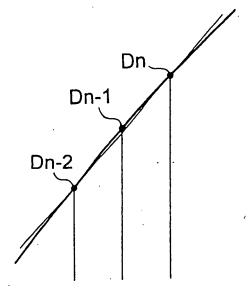


Fig.37

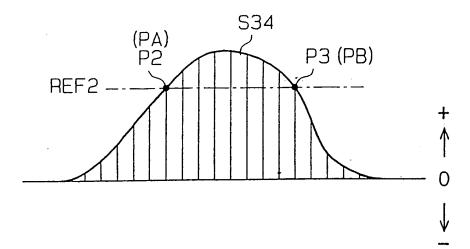


Fig.38

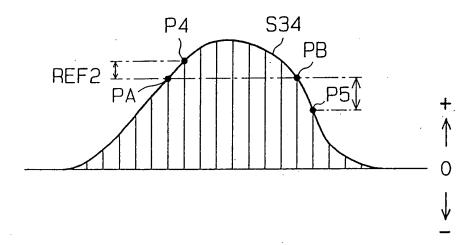
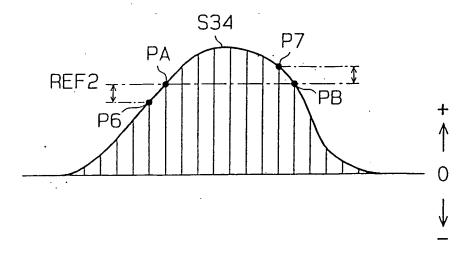


Fig.39



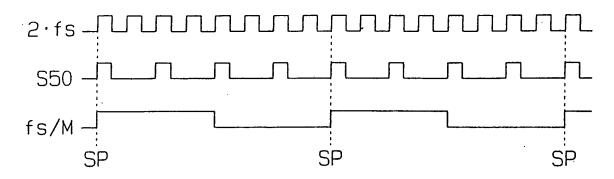


Fig.40B

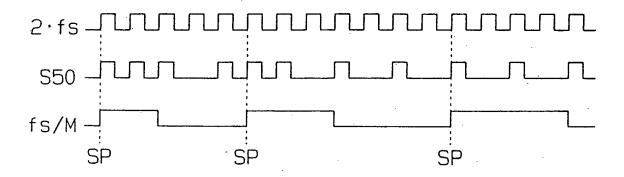
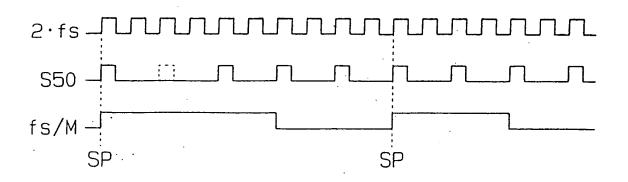


Fig.40C



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